IN THE CLAIMS

1. (Currently Amended) An apparatus for transmitting packets of data concurrently between a plurality of devices, comprising:

a switching matrix having a plurality of ports programmed to route packets from a source port to one of several destination ports, wherein the packets are comprised of a command word containing information corresponding to packet routing, data format, size, and transaction identification;

a first device coupled to the switching matrix;

a second device coupled to the switching matrix;

a third device coupled to the switching matrix, wherein the third device can transmit a first packet to the first device or the second device while the second device transmits a second packet to either the first device or the third device and while the first device transmits a third packet to either the second device or the third device, wherein each packet includes a coherent transaction bit that determines whether a packet is to be included in a coherent memory operation.

2. (Original) The apparatus of Claim 1, wherein the command word includes a destination identification number for routing the packet to a destination device.

3. (Original) The apparatus of Claim 1, wherein the command word includes a source identification number used by a destination device to send back responses.

4. (Original) The apparatus of Claim 1, wherein the command word includes a transaction number to tag requests that require a response.

5. (Original) The apparatus of Claim 1, wherein the command word includes a packet type value indicating a particular type of packet.

6. (Currently Amended) The apparatus of Claim 1, wherein ~~request packets include a bit that indicates a coherent transaction~~ each packet is one of a request packet and a response packet, the request packet operable to initiate an operation to take place, the response packet operable to provide a reply for a request packet.

7. (Original) The apparatus of Claim 1, wherein the command word includes a bit to guarantee bandwidth.

8. (Original) The apparatus of Claim 1, wherein the command word includes an error bit which indicates whether an error occurred during transmission.

9. (Original) The apparatus of Claim 1, wherein the command word includes a bit that is used as a sync barrier for write ordering.

10. (Original) The apparatus of Claim 1, wherein a packet corresponds to a fetch and operation packet with increment by one.

11. (Original) The apparatus of Claim 1, wherein a packet corresponds to a fetch and operation packet with decrement by one.

12. (Original) The apparatus of Claim 1, wherein a packet corresponds to a fetch and operation packet with clear.

13. (Original) The apparatus of Claim 1, wherein a packet corresponds to a store and operation packet with increment by one.

14. (Original) The apparatus of Claim 1, wherein a packet corresponds to a store and operation packet with decrement by one.

15. (Original) The apparatus of Claim 1, wherein a packet corresponds to a store and operation packet with a logical OR.

16. (Original) The apparatus of Claim 1, wherein a packet corresponds to a store and operation packet with a logical AND.

17. (Original) The apparatus of Claim 1, wherein a packet corresponds to a special packet.

18. (Original) The apparatus of Claim 1, wherein a packet includes sideband bits which are used to transfer information between sending and receiving devices.

19. (Currently Amended) A method for transmitting packets of data concurrently between a plurality of devices, comprising the steps of:

programming a switching matrix having a plurality of ports to route packets from a source port to one of several destination ports, wherein the packets are comprised of a command word containing information corresponding to packet routing, data format, size, and transaction identification;

transmitting data packets between a first device, a second device, and a third device coupled to the switching matrix as follows:

transmitting a first packet from the first device to the second or third device concurrently with;

transmitting a second packet from the second device to either the first device or the third device, concurrently with;

transmitting a third packet from the third device to either the first device or the third device;

wherein one of the data packets includes a virtual backplane bit.

20. (Original) The method of Claim 19, wherein the command word includes a destination identification number for routing the packet to a destination device, a source identification number used by a destination device to send back responses, a transaction number to tag requests that require a response, and a packet type value indicating a particular type of packet.

21. (Currently Amended) The method of Claim 19, wherein one of the data packets includes a bit that indicates a coherent transaction, a bit to guarantee bandwidth, ~~a virtual backplane bit,~~ an error bit which indicates whether an error occurred during transmission, and a bit that is used as a sync barrier for write ordering.

22. (Original) The method of Claim 19, wherein the packets correspond to a fetch and operation packet with increment by one, a fetch and operation packet with decrement by one, a fetch and operation packet with clear, a store and operation packet with increment by one, a store and operation packet with decrement by one, a store and operation packet with a logical OR, and a store and operation packet with a logical AND.

23. (Original) The method of Claim 19, wherein one of the packets includes sideband bits that are used to transfer information between sending and receiving devices.